

AVERAGE of time					branch		workers								patched							
WAL	size	m	machine	indexes	master	patched																
					0	0	1	2	3	4	6	8	0	1	2	3	4	6	8			
logged	small	100	i5	0	3.90	3.91	2.94	3.06	3.03	3.72	3.52	3.30	100%	75%	78%	78%	95%	90%	84%			
				1	8.78	8.17	7.66	7.58	7.34	9.00	8.70	9.08	93%	87%	86%	84%	103%	99%	103%			
				2	13.86	13.68	9.67	9.52	9.38	11.29	10.96	11.18	99%	70%	69%	68%	81%	79%	81%			
				3	19.52	18.57	15.61	12.40	12.47	14.51	14.54	14.37	95%	80%	64%	64%	74%	75%	74%			
				4	25.45	25.32	18.15	18.72	14.90	16.95	16.57	16.51	99%	71%	74%	59%	67%	65%	65%			
				5	33.31	30.54	26.13	21.98	21.82	20.47	20.79	19.32	92%	78%	66%	66%	61%	62%	58%			
			xeon	0	3.60	3.45	2.98	3.07	2.91	3.32	2.95	2.99	96%	83%	85%	81%	92%	82%	83%			
				1	6.82	6.25	6.78	5.93	6.19	5.89	5.54	5.71	92%	99%	87%	91%	86%	81%	84%			
				2	10.14	8.95	7.02	7.23	7.11	6.94	10.70	6.98	88%	69%	71%	70%	68%	106%	69%			
				3	12.66	11.65	10.51	9.05	8.02	7.85	8.17	7.67	92%	83%	72%	63%	62%	65%	61%			
				4	15.80	14.97	12.16	14.00	10.68	10.62	9.70	9.72	95%	77%	89%	68%	67%	61%	62%			
				5	23.52	18.67	15.27	15.92	13.42	12.15	11.73	15.82	79%	65%	68%	57%	52%	50%	67%			
				500	i5	0	3.70	3.70	1.83	1.77	1.73	2.24	2.05	1.98	100%	49%	48%	47%	61%	55%	53%	
						1	7.67	7.73	5.93	5.87	5.68	6.62	6.59	6.50	101%	77%	76%	74%	86%	86%	85%	
						2	11.37	11.28	6.85	6.79	6.67	7.48	7.57	7.40	99%	60%	60%	59%	66%	67%	65%	
	3	15.51	15.37			11.21	8.56	8.47	9.39	9.33	9.16	99%	72%	55%	55%	61%	60%	59%				
	4	19.81	19.76			12.90	12.92	9.62	10.40	10.27	10.12	100%	65%	65%	49%	53%	52%	51%				
	xeon	5	24.45	23.77	17.29	14.57	14.13	11.33	11.19	11.13	97%	71%	60%	58%	46%	46%	46%					
		0	3.26	3.32	1.83	1.81	1.71	1.84	1.84	1.81	102%	56%	56%	52%	56%	56%	55%					
		1	5.75	5.68	6.51	4.41	4.17	4.23	4.40	4.50	99%	113%	77%	73%	74%	77%	78%					
		2	7.70	7.91	5.14	4.82	4.62	4.78	4.65	5.02	103%	67%	63%	60%	62%	60%	65%					
		3	10.05	10.17	7.19	5.65	5.80	5.41	7.48	5.61	101%	71%	56%	58%	54%	74%	56%					
		4	12.33	11.70	8.40	8.66	6.99	6.58	6.67	8.76	95%	68%	70%	57%	53%	54%	71%					
		5	14.53	14.08	10.02	8.91	9.57	7.62	7.42	7.44	97%	69%	61%	66%	52%	51%	51%					
		1000	i5	0	3.12	3.19	0.91	0.88	0.87	1.13	1.07	0.96	102%	29%	28%	28%	36%	34%	31%			
				1	6.05	6.17	4.12	4.21	3.94	4.47	4.47	4.43	102%	68%	70%	65%	74%	74%	73%			
				2	8.88	8.98	4.69	4.60	4.55	5.08	5.06	4.94	101%	53%	52%	51%	57%	57%	56%			
	3			11.65	11.72	7.77	5.01	4.96	5.42	5.37	5.46	101%	67%	43%	43%	46%	46%	47%				
	4			14.58	14.52	8.66	8.28	5.29	5.71	5.78	5.71	100%	59%	57%	36%	39%	40%	39%				
	5			18.02	17.72	11.81	9.04	8.56	6.18	6.06	6.24	98%	65%	50%	47%	34%	34%	35%				
xeon	0		2.77	2.74	0.82	0.88	0.85	0.94	0.93	0.96	99%	29%	32%	31%	34%	34%	34%					
	1		4.60	4.51	2.85	2.88	2.81	2.84	2.84	2.91	98%	62%	63%	61%	62%	62%	63%					
	2		6.02	5.87	2.97	3.33	3.05	3.03	3.04	2.97	98%	49%	55%	51%	50%	51%	49%					
	3		10.15	7.52	4.77	3.57	3.42	3.44	3.42	3.31	74%	47%	35%	34%	34%	34%	33%					
	4		9.34	9.03	5.04	5.25	3.60	3.54	3.67	8.03	97%	54%	56%	39%	38%	39%	86%					
	5		11.39	11.07	7.21	5.47	5.61	4.96	3.91	4.02	97%	63%	48%	49%	44%	34%	35%					
	5000		i5	0	2.58	2.75	0.17	0.19	0.16	0.24	0.20	0.19	107%	6%	7%	6%	9%	8%	7%			
				1	4.38	4.47	2.36	2.33	2.31	2.40	2.42	2.44	102%	54%	53%	53%	55%	55%	56%			

				2	6.24	6.17	2.72	2.68	2.68	2.80	2.84	2.73	99%	44%	43%	43%	45%	45%	44%
				3	7.86	7.87	4.85	2.98	3.01	3.02	3.02	3.03	100%	62%	38%	38%	38%	38%	39%
				4	9.65	9.69	5.38	5.10	3.08	3.13	3.14	3.10	100%	56%	53%	32%	32%	33%	32%
				5	11.50	11.47	7.44	5.48	5.27	3.38	3.37	3.38	100%	65%	48%	46%	29%	29%	29%
			xeon	0	2.34	2.32	0.16	0.18	0.16	0.16	0.18	0.19	99%	7%	7%	7%	7%	7%	8%
				1	3.61	3.56	1.84	1.80	1.90	1.74	1.79	1.76	99%	51%	50%	53%	48%	50%	49%
				2	4.72	4.73	1.85	1.83	1.84	1.84	1.89	1.92	100%	39%	39%	39%	39%	40%	41%
				3	5.88	6.07	3.38	2.01	1.95	1.95	2.02	1.95	103%	58%	34%	33%	33%	34%	33%
				4	7.05	7.19	3.45	3.50	2.02	2.00	2.03	2.03	102%	49%	50%	29%	28%	29%	29%
				5	8.46	8.37	5.06	3.63	3.66	2.13	2.25	2.13	99%	60%	43%	43%	25%	27%	25%
unlogged	small	100	i5	0	3.06	3.01	1.67	1.11	0.90	0.87	0.88	0.91	98%	55%	36%	30%	29%	29%	30%
				1	6.95	6.82	4.52	3.72	3.31	3.47	3.35	3.40	98%	65%	54%	48%	50%	48%	49%
				2	9.31	8.98	4.77	4.11	3.70	3.81	3.79	3.88	96%	51%	44%	40%	41%	41%	42%
				3	11.43	11.14	7.30	4.24	4.17	4.08	4.18	4.24	97%	64%	37%	36%	36%	37%	37%
				4	13.82	13.81	7.88	6.91	4.44	4.49	4.59	4.45	100%	57%	50%	32%	32%	33%	32%
				5	16.70	16.38	10.26	7.22	7.27	5.51	5.53	5.62	98%	61%	43%	44%	33%	33%	34%
			xeon	0	2.60	2.52	1.51	1.17	0.95	0.85	0.75	0.74	97%	58%	45%	37%	33%	29%	29%
				1	5.81	5.91	4.12	3.52	3.14	3.21	2.94	2.73	102%	71%	61%	54%	55%	51%	47%
				2	7.57	7.36	4.27	3.85	3.50	3.35	3.05	3.05	97%	56%	51%	46%	44%	40%	40%
				3	9.30	9.75	6.52	4.02	3.66	3.62	3.43	3.14	105%	70%	43%	39%	39%	37%	34%
				4	12.00	11.77	6.84	6.20	4.08	3.78	3.74	3.25	98%	57%	52%	34%	32%	31%	27%
				5	14.81	15.17	9.52	6.37	6.23	4.04	3.59	3.42	102%	64%	43%	42%	27%	24%	23%
		500	i5	0	3.00	3.10	0.88	0.61	0.47	0.48	0.48	0.48	103%	29%	20%	16%	16%	16%	16%
				1	5.86	5.99	3.15	2.82	2.60	2.69	2.68	2.71	102%	54%	48%	44%	46%	46%	46%
				2	7.30	7.62	3.61	3.07	2.88	2.88	2.90	2.87	104%	49%	42%	39%	39%	40%	39%
				3	9.40	10.22	5.40	3.22	3.18	3.19	3.20	3.15	109%	58%	34%	34%	34%	34%	33%
				4	12.19	12.42	6.13	5.38	4.23	3.99	3.75	3.65	102%	50%	44%	35%	33%	31%	30%
				5	12.82	13.32	7.76	7.04	7.08	6.76	6.87	7.00	104%	61%	55%	55%	53%	54%	55%
			xeon	0	2.64	2.64	0.78	0.60	0.49	0.41	0.35	0.34	100%	30%	23%	18%	16%	13%	13%
				1	4.79	4.91	2.92	2.60	2.55	2.47	2.44	2.18	103%	61%	54%	53%	52%	51%	46%
				2	6.35	6.07	3.04	2.87	2.47	2.54	2.38	2.23	96%	48%	45%	39%	40%	38%	35%
				3	7.85	7.87	4.61	2.81	2.78	2.53	2.53	2.54	100%	59%	36%	35%	32%	32%	32%
				4	8.89	9.35	4.97	4.70	2.83	2.72	2.77	2.44	105%	56%	53%	32%	31%	31%	27%
				5	10.93	11.05	6.52	4.83	4.61	2.69	2.66	2.49	101%	60%	44%	42%	25%	24%	23%
		1000	i5	0	2.77	2.92	0.45	0.32	0.25	0.25	0.25	0.26	105%	16%	12%	9%	9%	9%	9%
				1	4.54	4.64	2.27	2.08	1.99	2.05	2.02	2.13	102%	50%	46%	44%	45%	45%	47%
				2	5.85	5.97	2.43	2.33	2.12	2.19	2.18	2.21	102%	41%	40%	36%	37%	37%	38%
				3	7.93	8.29	4.09	2.32	2.21	2.26	2.26	2.28	105%	52%	29%	28%	29%	29%	29%
				4	8.60	9.35	4.51	4.06	2.31	2.44	2.36	2.36	109%	52%	47%	27%	28%	27%	27%
				5	10.12	10.07	6.15	5.03	4.08	3.30	3.05	3.09	100%	61%	50%	40%	33%	30%	31%
			xeon	0	2.50	2.49	0.40	0.32	0.26	0.22	0.20	0.18	100%	16%	13%	10%	9%	8%	7%

				1	4.12	4.08	2.12	2.01	1.94	1.88	1.84	1.72	99%	51%	49%	47%	46%	45%	42%
				2	5.18	5.28	2.13	2.11	1.96	1.86	1.82	1.79	102%	41%	41%	38%	36%	35%	35%
				3	6.53	6.54	3.71	2.13	2.09	1.97	1.99	1.97	100%	57%	33%	32%	30%	30%	30%
				4	8.18	7.46	3.71	3.61	2.22	2.17	2.04	1.96	91%	45%	44%	27%	26%	25%	24%
				5	9.69	8.70	5.41	3.63	3.57	2.10	1.98	2.01	90%	56%	37%	37%	22%	20%	21%
		5000	i5	0	2.61	2.76	0.11	0.08	0.07	0.07	0.07	0.07	106%	4%	3%	3%	3%	3%	3%
				1	3.88	3.99	1.75	1.67	1.67	1.66	1.70	1.68	103%	45%	43%	43%	43%	44%	43%
				2	5.09	5.14	1.83	1.81	1.86	1.78	1.81	1.91	101%	36%	36%	37%	35%	36%	38%
				3	6.23	6.30	3.40	1.98	1.93	1.86	1.90	1.86	101%	55%	32%	31%	30%	30%	30%
				4	7.44	8.14	3.51	3.43	1.90	1.93	2.07	1.94	109%	47%	46%	26%	26%	28%	26%
				5	8.58	8.62	5.08	3.54	3.51	2.42	2.47	2.47	100%	59%	41%	41%	28%	29%	29%
			xeon	0	2.44	2.40	0.10	0.08	0.07	0.06	0.06	0.06	98%	4%	3%	3%	3%	2%	2%
				1	3.59	3.58	1.70	1.60	1.65	1.53	1.55	1.55	100%	47%	45%	46%	43%	43%	43%
				2	4.59	4.72	1.71	1.62	1.72	1.57	1.55	1.60	103%	37%	35%	37%	34%	34%	35%
				3	5.80	5.79	3.11	1.71	1.68	1.68	1.67	1.75	100%	54%	29%	29%	29%	29%	30%
				4	6.71	6.87	3.27	3.10	1.93	1.76	1.70	1.77	102%	49%	46%	29%	26%	25%	26%
				5	7.83	8.04	4.71	3.13	3.24	1.93	1.76	1.99	103%	60%	40%	41%	25%	23%	25%